AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all previous listings and versions of claim in this application.

1. (Original) A method for minimizing slip line faults on a surface of a semiconductor wafer that has been obtained using a transfer technique, which comprises:

heating such semiconductor wafer from an ambient temperature to a first higher temperature;

pausing the heating at the first higher temperature for a time sufficient to stabilize the wafer; and

further heating the wafer from the first higher temperature to a target higher temperature during a predetermined time interval, with the further heating during an initial portion of the time interval being conducted at a relatively low heating rate and heating during a final portion of the time interval being conducted at a relatively higher heating rate to thus minimize slip line faults in the surface of the wafer.

2. (Original) The method of claim 1 wherein the further heating during the predetermined time interval is not uniform and overall is less than 50°C/sec.

3. (Original) The method of claim 2 wherein the further heating continuously increases from the low heating rate to the high heating rate.

4. (Original) The method of claim 3 wherein the low heating rate is conducted from more than 50% to about 80% of the predetermined time interval and the high heating rate is conducted from about less than 50% to about 20% of the predetermined time interval.

5. (Original) The method of claim 1 which further comprises pausing the heating during the initial portion of the time interval and then resuming heating.

6. (Original) The method of claim 1 wherein the ambient temperature is room temperature and the first higher temperature is about 700 to 800°C.

7. (Original) The method of claim 1 wherein the low heating rate of the further heating is conducted from the first higher temperature to an intermediate temperature of between about 800 to about 1100°C, and the high heating rate of the further heating is conducted from the intermediate temperature to the target temperature.

8. (Original) The method of claim 1 wherein the target temperature is about 1100 to 1300°C.

9. The method of claim 1 wherein the high heating rate of the further heating is about 25 to 50°C per second.

10. (Original) The method of claim 1 wherein the wafer is made of silicon.

11. (Original) The method of claim 1 wherein the wafer is an SOI wafer.

12. (Original) A method for minimizing slip line faults on a surface of a semiconductor wafer that has been obtained using a transfer technique, which comprises:

heating such semiconductor wafer from an ambient temperature to a first higher temperature of about 700 to 800°C;

halting the heating at the first higher temperature for a time sufficient to stabilize the wafer; and

further heating the wafer from the first higher temperature to a target higher temperature of about 1100 to 1300°C during a predetermined time interval, with the further heating during an initial portion of the time interval being conducted continuously at a relatively low heating rate from the first higher temperature to an intermediate temperature of about 800 to 1100°C and at a relatively higher heating rate during a final portion of the time interval to the target temperature to thus minimize slip line faults in the surface of the wafer.

13. (Original) The method of claim 12 wherein the low heating rate is conducted from more than 50% to about 80% of the predetermined time interval and the high heating rate is conducted from less than 50% to about 20% of the predetermined time interval.

14. (Original) The method of claim 12 which further comprises pausing the heating during the initial portion of the time interval and then resuming heating.

15. (Original) The method of claim 12 wherein the first higher temperature is around 750°C and the target temperature is in the range of about 1150 to 1250°C.

16. (Original) The method of claim 12 wherein the high heating rate of the further heating is about 25 to 50°C per second.

17. (Original) The method of claim 12 wherein the wafer is made of silicon.

18. (Original) The method of claim 12 wherein the wafer is an SOI wafer.

19. (Original) In a method for minimizing slip line faults on a surface of a semiconductor wafer that has been obtained using a transfer technique, wherein the wafer has been heated from an ambient temperature to a first higher temperature and a pause has been taken at the first higher temperature for a time sufficient to stabilize the wafer, the improvement comprising further heating the wafer from the first higher temperature to a target higher temperature during a predetermined time interval, with the further heating during an initial portion of the time interval being conducted at a relatively low heating rate and heating during a final portion of the time interval being conducted at a relatively higher heating rate to thus minimize slip line faults in the surface of the wafer.

20. (New) A method for minimizing slip line faults on a surface of a semiconductor wafer that has been obtained using a transfer technique, which comprises:

heating such semiconductor wafer from an ambient temperature to a first higher temperature;

pausing the heating at the first higher temperature for a time sufficient to stabilize the wafer; and

further heating the wafer from the first higher temperature to a target higher temperature during a predetermined time interval, with the further heating during the time interval being conducted at a non-rectilinear heating rate to thus minimize slip line faults in the surface of the wafer.